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REMARKS/ARGUMENTS

Claims 1-15 are pending in the present application. With this amendment, claims 1 and 8 have been amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 103(a), Obviousness

I.A Claims 1, 2, 5-6, 8-9 and 12-13 over *Nance* in view of *Conner*

The examiner has rejected claims 1, 2, 5-6, 8-9 and 12-13 under 35 U.S.C. § 103(a) as being unpatentable over *Nance* et al., Multiport RAM with Programmable Data Port Configuration, U.S. Patent No. 5,715,197 (February 3, 1998) (hereinafter "*Nance*") in view of *Conner*, Tester for LSI Devices and Memory Devices, U.S. Patent No. 4,450,560 (May 22, 1984) (hereinafter "*Conner*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants have amended the independent claims, claims 1 and 8, to describe the mapping logic mapping one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups. Some examples of support for this amendment can be found in Applicants' specification on page 5, lines 2-3; page 7, lines 16-17; page 10, lines 4-7; and Figure 5.

The Examiner asserts that *Nance* teaches the features of Applicants' independent claims but fails to teach chip testing and test signal groups. The Examiner relies on *Conner* to cure the deficiencies of *Nance*. The combination of *Nance* and *Conner* does not render Applicants' claims obvious because the combination does not teach or suggest mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups.

Nance teaches RAM that is used for storing data that includes data ports that have a programmably configurable data width. Four input signals are supplied to each one of the RAM's input ports. The four signals are received by four input multiplexers, such that each one of the input multiplexers receives the same four signals. For example, see *Nance*, Figure 2: multiplexers 203, 205, 207, and 209. A decoder is used to select one of the input multiplexers' inputs. The selected inputs are corresponding inputs in each multiplexer. The decoder selects the I0, I1, I2, or I3 inputs. See *Nance*, Figure 2. When the I1 input is selected, for example, the I1 input in all input multiplexers is selected.

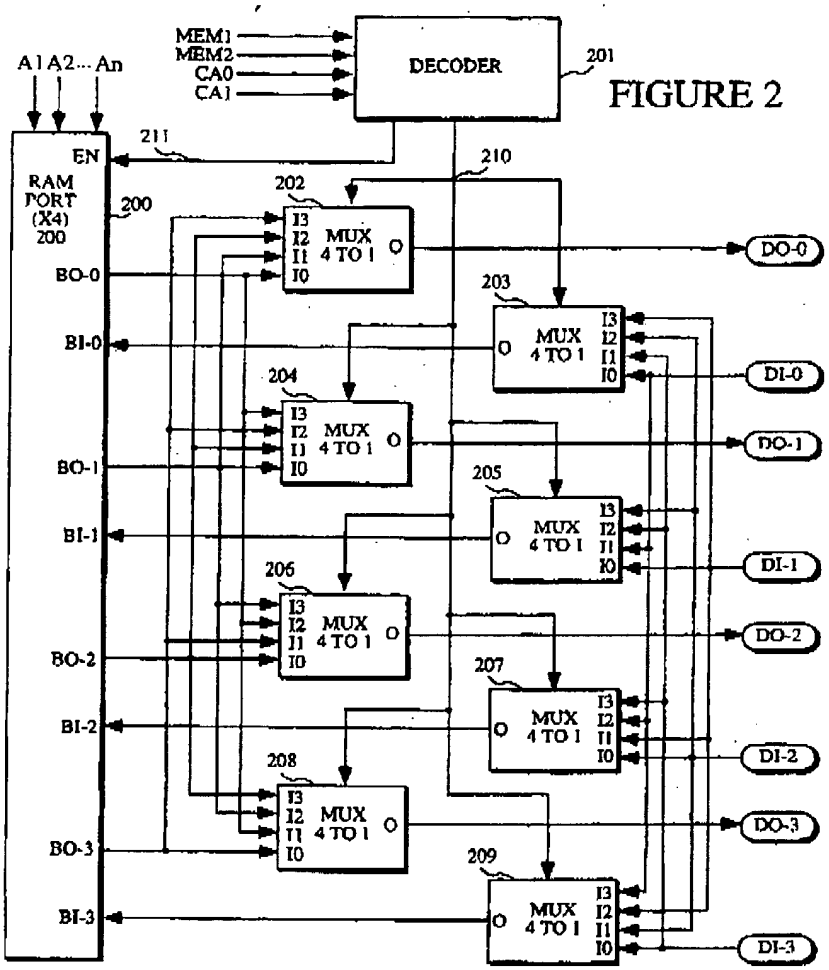

FIGURE 2

Nance, Figure 2.

When one of the input multiplexers' four inputs is selected, one of the four input signals is selected. For example, when the I0 input is selected, a first input multiplexer selects the D0 signal, a second input multiplexer selects the D1 signal, a third input multiplexer selects the D2 signal, and a fourth input multiplexer selects the D3 signal. The data from each selected input signal is then received by and stored within the RAM.

Each one of the RAM's ports has four outputs, each output generating one output signal. There are four output multiplexers. For example, see *Nance*, Figure 2: multiplexers 202, 204, 206, and 208. Each output multiplexer has four inputs, each input for receiving a different one of the output signals. Thus, each one of the four output signals is received by one, and only one, of the four inputs of each

multiplexer. Therefore, the same output signal is not mapped to at least two of the inputs of any output multiplexer.

In *Nance*, each signal is mapped to only one input of a multiplexer. Each multiplexer has four inputs, and receives four different signals. Each input multiplexer receives signals D0, D1, D2, and D3. Each output multiplexer receives signals B0, B1, B2, and B3. Therefore, nothing in *Nance* teaches one signal that is mapped to two outputs of mapping logic concurrently to output as two different signals.

The Examiner stated that *Nance* does not teach chip testing or test signal groups and relies on *Conner* to cure the deficiencies of *Nance*. *Conner* does not cure the deficiencies of *Nance*, however, because *Conner* does not teach mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups.

Because the combination of *Nance* and *Conner* does not teach or suggest mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups, the combination of *Nance* and *Conner* does not render Applicants' claims obvious. Therefore, the rejection of claims 1, 2, 5-6, 8-9 and 12-13 under 35 U.S.C. § 103(a) has been overcome.

I.B Claims 3 and 10 over *Nance* and *Conner* in view of *Swart*

The examiner has rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Nance* and *Conner*, and further in view of *Swart*, Expandable Diaphragm Test Modules and Connectors, U.S. Patent No. 5,389,885 (February 14, 1995) (hereinafter "*Swart*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants' claims 3 and 10 describe concurrently observing test signals for a plurality of modules.

The Examiner stated:

> As per claim 3, Nance et al. and Conner substantially teach the claimed invention described in claim 2 (as rejected above).
>
> However Nance et al. and Conner do not explicitly teach the specific use of the method, further comprising: concurrently observing test signals for a plurality of modules.
>
> Swart in an analogous art teaches that electrical test signals ... under test (col. 8, line 65 to col. 9, line 2, Swart).

Office Action dated October 19, 2006, pages 4-5.

The combination of *Nance*, *Conner*, and *Swart* does not render Applicants' claims obvious because the combination does not teach or suggest mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups, in combination with concurrently observing test signals for a plurality of modules.. Therefore, the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) has been overcome.

I.C. Claims 4 and 11 over *Nance, Conner* and *Swart* in view of *Moore, et al.*

The examiner has rejected claims 4 and 11 under 35 U.S.C. § 103(a) as being unpatentable over *Nance, Conner*, and *Swart*, and further in view of *Moore* et al., Test Access Architecture for Testing of Circuits Modules at an Intermediate Node within an Integrated Circuit Chip, U.S. Patent No. 5,604,432 (February 18, 1997) (hereinafter "*Moore*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants' claims 4 and 11 describe wherein the plurality of modules includes identical modules. The Examiner stated:

> As per claim 4, Nance et al., Conner and Swart substantially teach the claimed invention described in claim 3 (as rejected above).
>
> However Nance et al., Conner and Swart do not explicitly teach the specific use of the method, wherein the plurality of modules includes identical modules.
>
> Moore et al. in an analogous art teach that it is desirable to be able to use the same test vectors for identical modules (col. 4, lines 43-44, Moore et al.).

Office Action dated October 19, 2006, pages 5-6.

The combination of *Nance*, *Conner*, *Swart*, *Moore* does not render Applicants' claims obvious because the combination does not teach or suggest mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups, in combination with wherein the plurality of modules includes identical modules. Therefore, the rejection of claims 4 and 11 under 35 U.S.C. § 103(a) has been overcome.

I.D. Claims 14 and 15 over *Nance* and *Conner* in view of *Wittig, et al.*

The examiner has rejected claims 14 and 15 under 35 U.S.C. § 103(a) as being unpatentable over *Nance* and *Conner*, and further in view of *Wittig* et al., Method for Implementing Large Multiplexers with FPGA Lookup Tables, U.S. Patent No. 6,118,300 (September 12, 2000) (hereinafter "*Wittig*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants' claims 14 and 15 describe mapping, by said mapping logic, a first one of said plurality of test signal groups, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first test output group;

mapping, by said mapping logic, a second one of said plurality of test signal groups, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second test output group; and

said first one of said plurality of test signal groups and said second one of said plurality of test signal groups being a same signal type of signal.

The Examiner stated that the combination of *Nance* and *Conner* substantially teaches the claimed invention. The Examiner relies on *Wittig* to cure the deficiencies of the combination of *Nance* and *Conner*.

The combination of *Nance, Conner*, and *Wittig* does not render Applicants' claims 14 and 15 obvious because the combination does not teach or suggest mapping logic that maps one of the plurality of test signal groups to at least two of the plurality of outputs of the mapping logic concurrently to output as two different test output groups, in combination with the features of claims 14 and 15. Therefore, the rejection of claims 14 and 15 under 35 U.S.C. § 103(a) has been overcome.

II. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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